A 1.25Gbit/s Serializer for LHC Data and Trigger Optical Links

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Outline

- LHC high-speed optical links
- Serializer “primer”
- ASIC architecture:
  - High-speed serializer
  - Clock generator
  - Phase-locked loop
- Testing the IC
- Summary

LHC High-Speed Optical Links

- Gbit/s data links:
  - Sub-detectors ⇔ control/counting room
  - In data readout systems
    - Asynchronous data transmission is possible
  - In the trigger systems data path
    - Data transmission must be synchronous with the 40.08MHz LHC master clock

LHC High-Speed Optical Links

- Typical configuration:
  - Unidirectional
- Transmitters inside the detectors:
  - Transmitters subject to high levels of radiation during the experiments lifetime
  - Large numbers ⇒ constrained power consumption

LHC High-Speed Optical Links

- LHC high-speed links requirements:
  - Hardness to total dose radiation effects
  - Operation tolerant to SEU
  - Constant latency transmission for trigger systems (40.08 MHz synchronous)
  - Low power dissipation
  - Low cost

LHC High-Speed Optical Links

- Can commercial devices fulfil HEP requirements?
  - Bandwidth (Yes)
  - Constant latency transmission (Yes, ...)
  - Radiation tolerance (No)
  - Operation tolerant to SEU (No)
  - Low power (?)
  - Low cost (?)

LHC High-Speed Optical Links

- Radiation hardness: is there an alternative?
  - Specially hardened processes

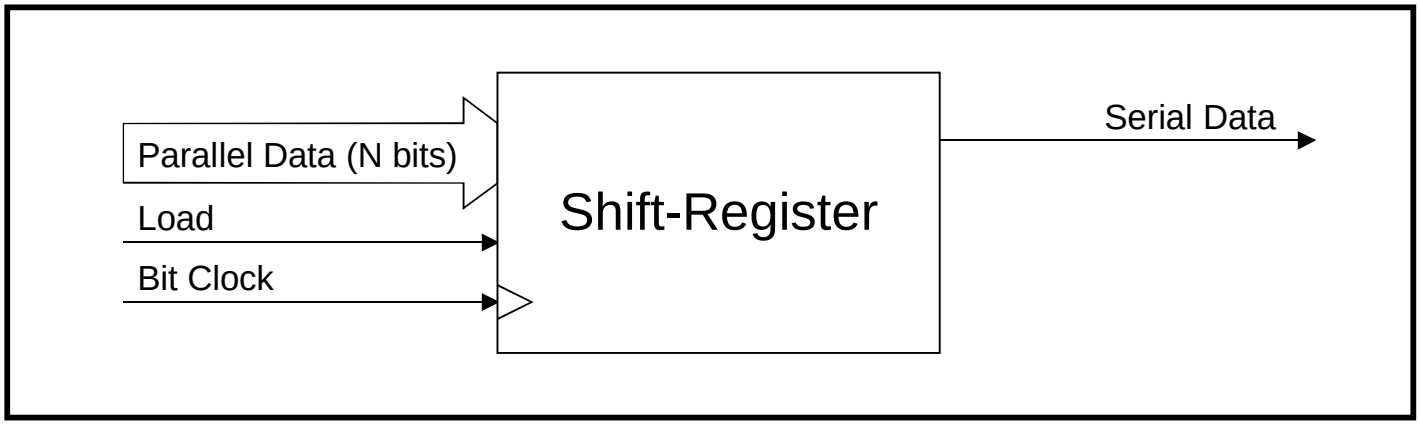
  OR
  - Mainstream sub-μm CMOS processes
    + radiation tolerant layout techniques

LHC High-Speed Optical Links

- Why sub-μm CMOS?
  - Today's semiconductor industry standard
  - Bandwidth capabilities exceed HEP requirements
  - Low power consumption
  - Price advantage when compared with any specially hardened technology
  - If used with radiation tolerant techniques
    - Very high resistance to total dose effects
    - Virtually single event latchup immune

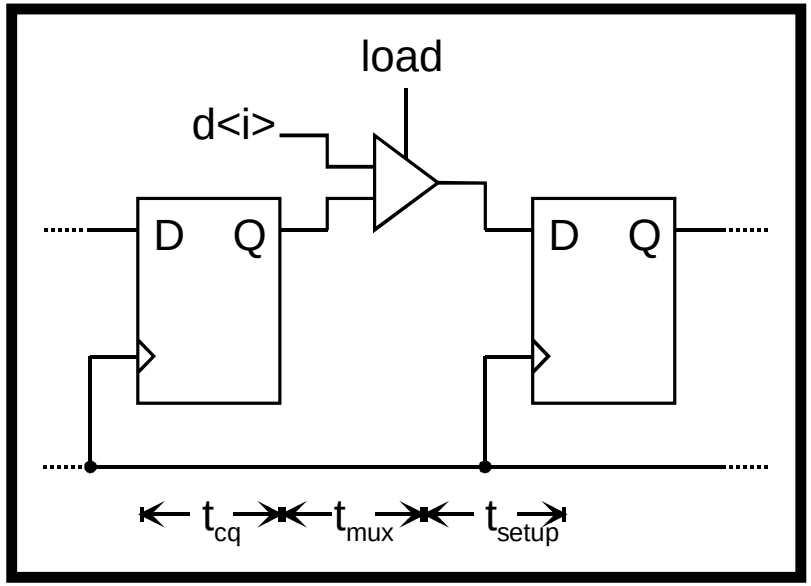
Serializer “Primer”

- What is a serializer?
  - A shift register!
  - Parallel loaded at the “word rate”
  - “Emptied” at the “bit rate”
  - “Bit rate” = (#bits in word) $\times$ (data rate)



Serializer “Primer”

- Parallel-load shift register:
  - cascade of flip-flops and 2-to-1 multiplexers
- Operation speed is limited by:
  - clock to Q delay
  - mux delay
  - flip-flop setup time
- Maximum frequency:
  - $1/(t_{cq} + t_{mux} + t_{setup})$

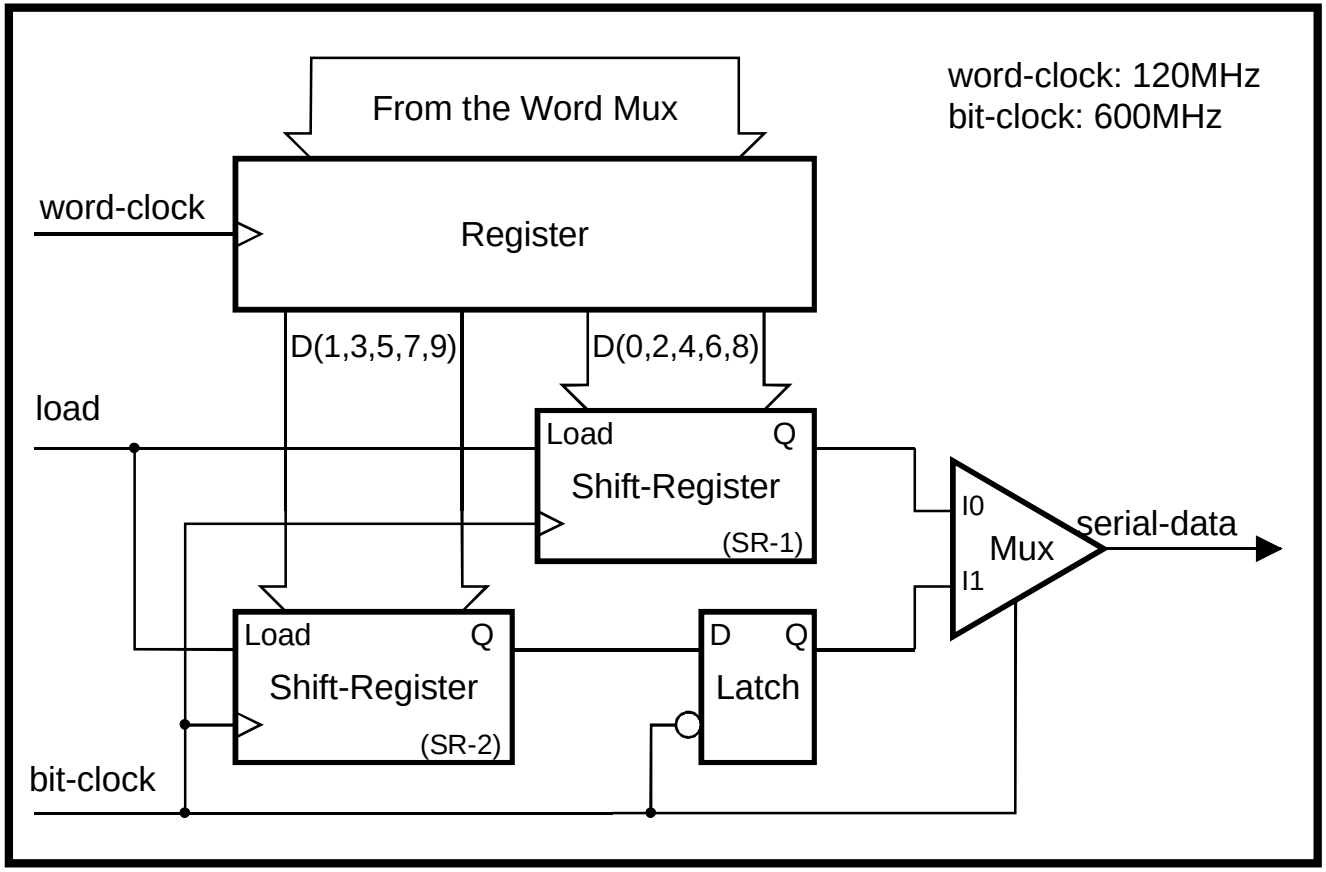


Serializer “Primer”

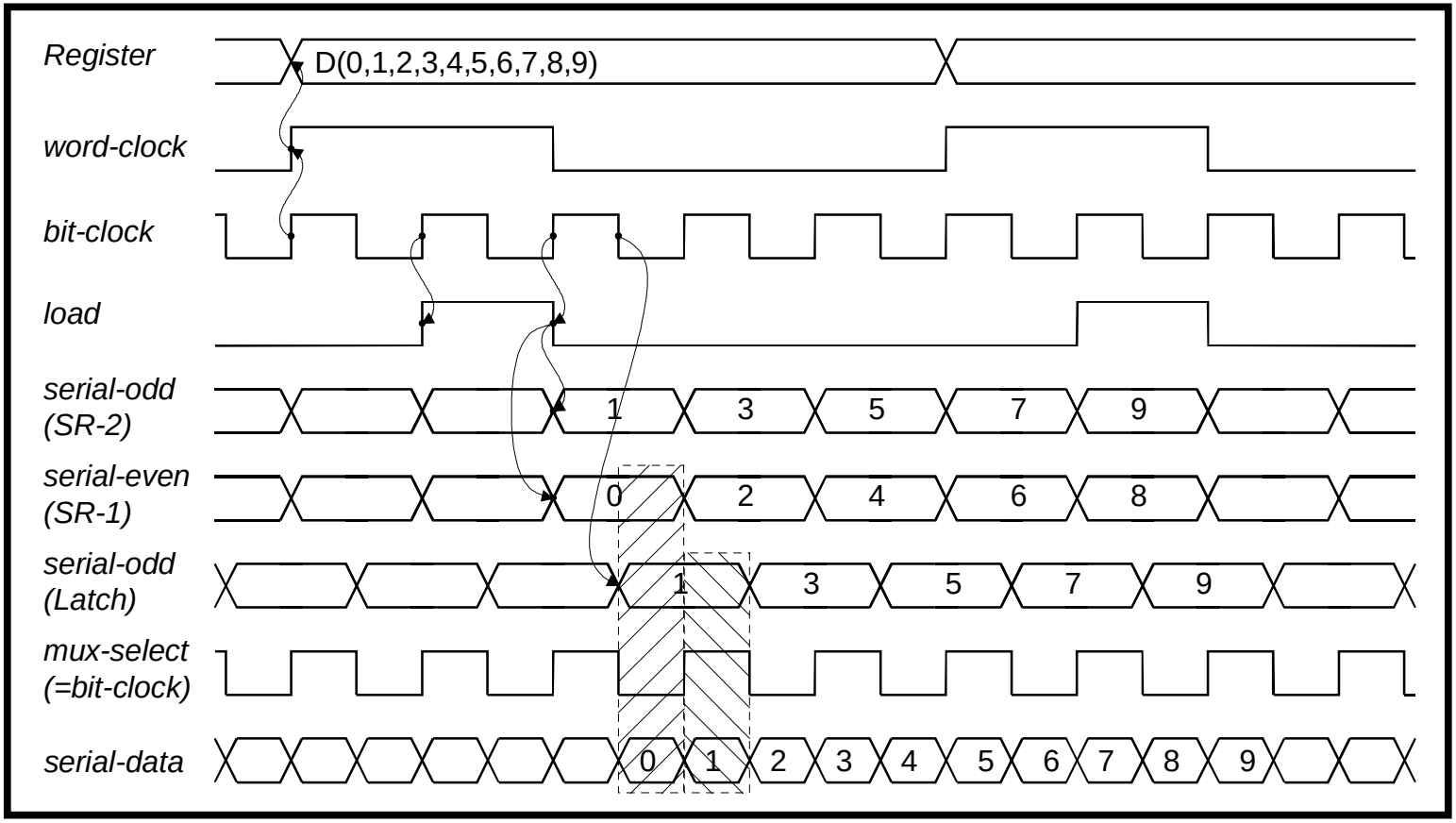
- Operation @ 1.25GHz ⇒ T = 800ps
- Static FF t(min) = 1292ps ! (worst case)
- Dynamic FF t(min) = 768ps (worst case)
- Can we use Dynamic FF?
  - **No, they are sensitive to SEU**

	DFF t_{pd} (ps)	DFF t_{sup} (ps)	SFF t_{pd} (ps)	SFF t_{sup} (ps)	MUX t_{pd} (ps)
typical	145	60	309	107	104
worst	369	152	749	296	247

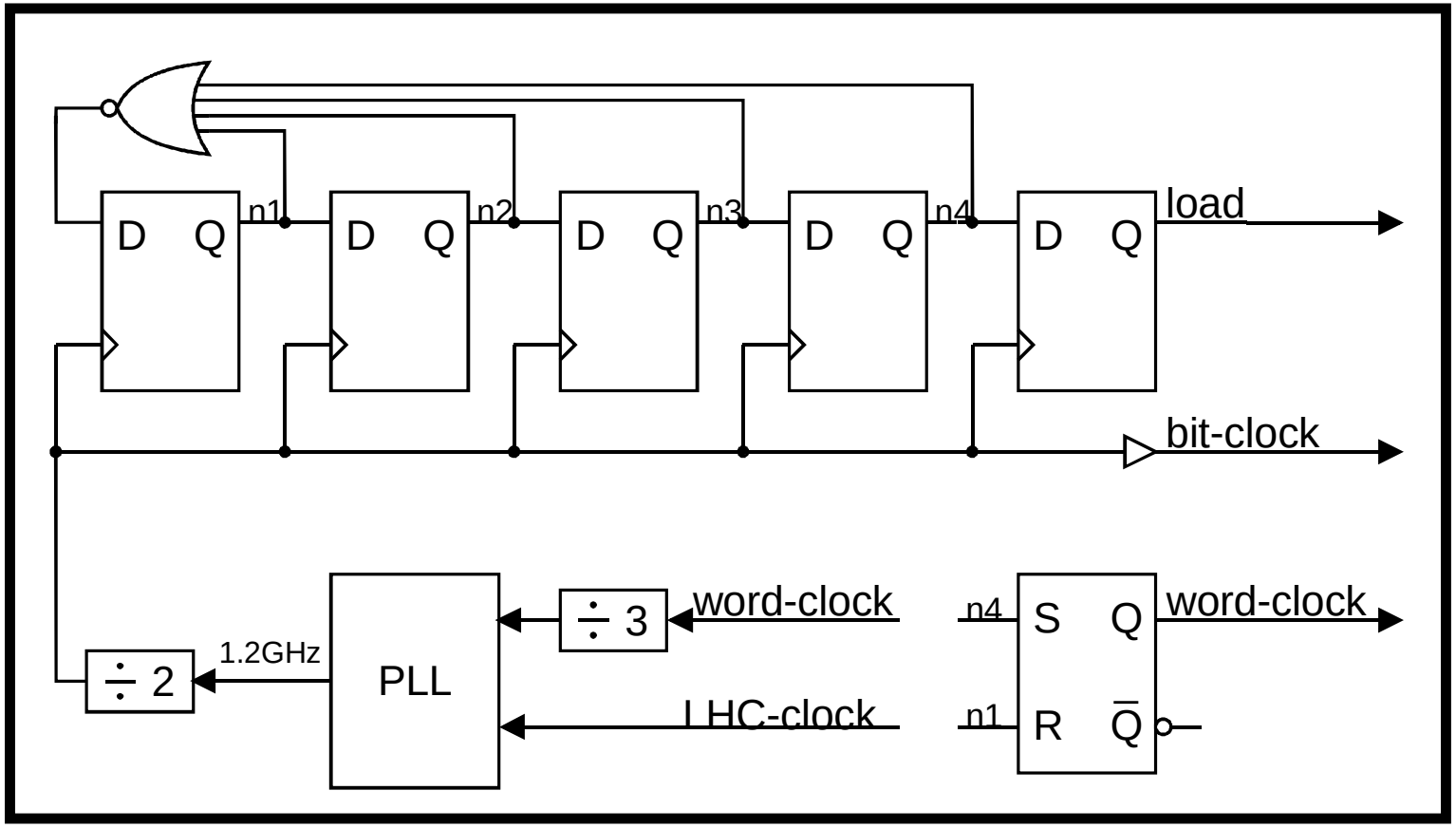
ASIC Architecture



ASIC Architecture



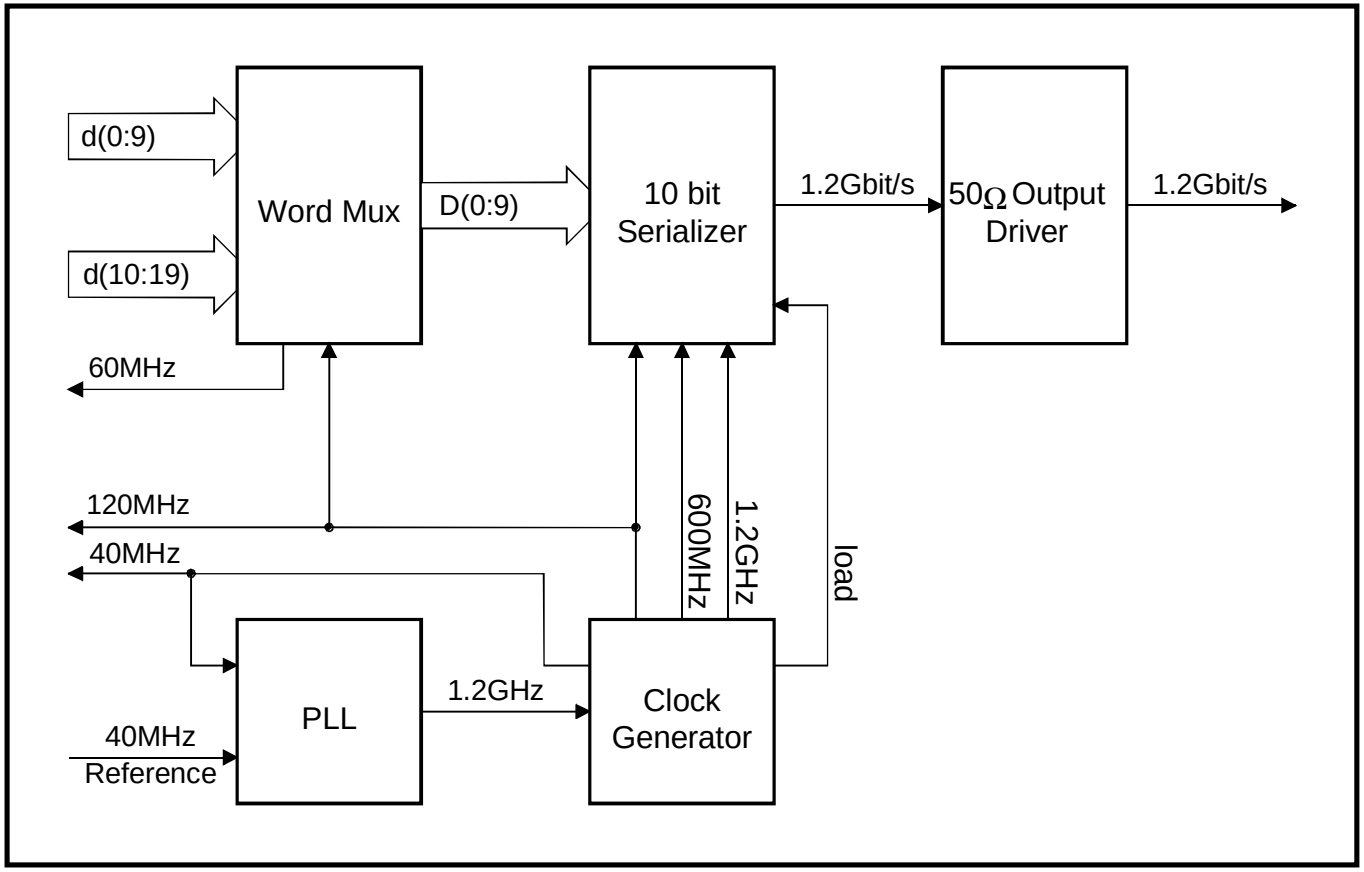
ASIC Architecture



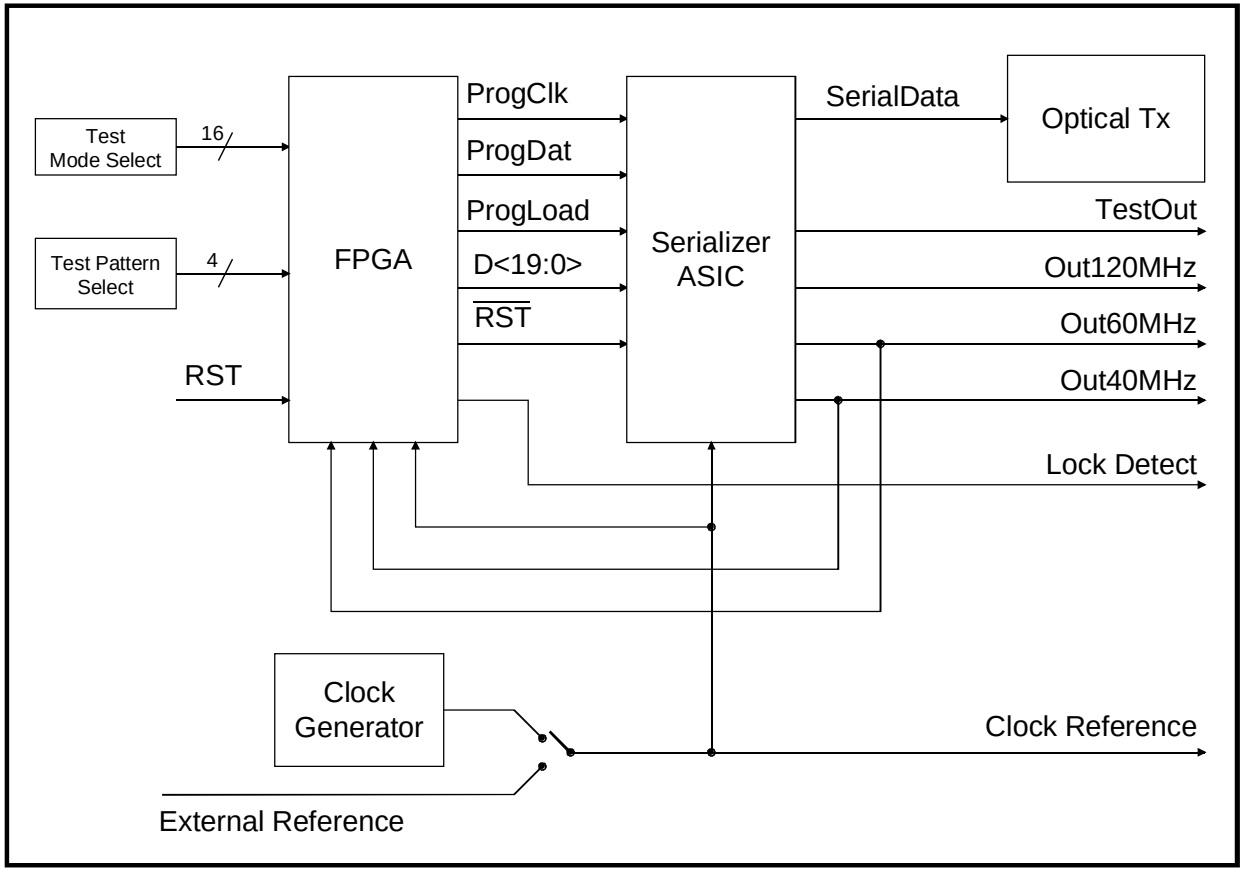
ASIC Architecture

- The PLL
  - Classical structure
  - Three-state phase-frequency detector
  - Charge-pump
  - RC loop filter
  - Three differential cells with symmetrical loads

ASIC Architecture



Testing the IC



Summary

- A 1.2GHz Serializer IC has been fabricated in 0.25μm CMOS
- The design uses radiation tolerant layout techniques
- A test setup has been developed using standard industrial components
- …