LOGIC STATE ANALYZER

CONTROL SIGNALS

J4 — CON64MLDC

LD<31..0>

LDERR	5	LDERR_N	
LDOWN	7	LDOWN_N	
LWEN	14	LWEN_N	
LCTRL	19	LCTRL_N	
LCLK	11	LCLK	
LD31	21	LD<31>	31
LD30	24	LD<30>	30
LD29	25	LD<29>	29
LD28	26	LD<28>	28
LD27	27	LD<27>	27
LD26	29	LD<26>	26
LD25	30	LD<25>	25
LD24	32	LD<24>	24
LD23	33	LD<23>	23
LD22	34	LD<22>	22
LD21	35	LD<21>	21
LD20	37	LD<20>	20
LD19	38	LD<19>	19
LD18	40	LD<18>	18
LD17	41	LD<17>	17
LD16	42	LD<16>	16
LD15	43	LD<15>	15
LD14	45	LD<14>	14
LD13	46	LD<13>	13
LD12	48	LD<12>	12
LD11	49	LD<11>	11
LD10	50	LD<10>	10
LD9	51	LD<9>	9
LD8	53	LD<8>	8
LD7	54	LD<7>	7
LD6	56	LD<6>	6
LD5	57	LD<5>	5
LD4	58	LD<4>	4
LD3	59	LD<3>	3
LD2	61	LD<2>	2
LD1	62	LD<1>	1
LD0	64	LD<0>	0

UXOFF_N	10	UXOFF	
URESET_N	15	URESET	
UTDO_N	18	UTDO	
UDW<1>	17	UDW1	
UDW<0>	20	UDW0	
URL<3>	1	URL3	
URL<2>	2	URL2	
URL<1>	4	URL1	
URL<0>	6	URL0	

VCC — SMD 6.8UF C12 — GND
VCC — SMD 6.8UF C11 — GND

J1 — VROUD2X10

LCLK	3	1	ST1
	5	1	ST2
LDERR_N	7	8	UXOFF_N
LDOWN_N	9	10	URESET_N
UTDO_N	11	12	LWEN_N
LCTRL_N	13	14	UDW<1>
UDW<0>	15	16	URL<3>
URL<2>	17	18	URL<1>
URL<0>	19	20	

GND

LD<31..0>

J3 — VROUD2X10 — LD<31..16>

30	LD<30>	5	6 LD<29> 29
28	LD<28>	7	8 LD<27> 27
26	LD<26>	9	10 LD<25> 25
24	LD<24>	11	12 LD<23> 23
22	LD<22>	13	14 LD<21> 21
20	LD<20>	15	16 LD<19> 19
18	LD<18>	17	18 LD<17> 17
16	LD<16>	19	20

GND

J2 — VROUD2X10 — LD<15..0>

14	LD<14>	5	6 LD<13> 13
12	LD<12>	7	8 LD<11> 11
10	LD<10>	9	10 LD<9> 9
8	LD<8>	11	12 LD<7> 7
6	LD<6>	13	14 LD<5> 5
4	LD<4>	15	16 LD<3> 3
2	LD<2>	17	18 LD<1> 1
0	LD<0>	19	20

GND

PATTERN TYPE

SW1 ERG10412

0	TEST PATTERN
1	WALKING ONE
2	WALKING ZERO
3	ADD - 1Ø
4	ADD - 5Ø
5	RANDOM
6	RANDOM NO CNTL
7	RANDOM ALL CNTL
8	ROB <1 LENGTH>
9	ROB <4 LENGTHS>

VCC — 1K R53 — SW_PATT8 15
VCC — 1K R55 — SW_PATT4 14
VCC — 1K R54 — SW_PATT2 13
VCC — 1K R52 — SW_PATT1 12

GND

DUTY TYPE

SW2 ERG10412

0	RUN
1	SINGLE STEP
2	SINGLE BLOCK
3	EVERY 2
4	EVERY 4
5	EVERY 8
6	EVERY 16
7	EVERY 32
8	EVERY 64
9	EVERY 128

VCC — 1K R57 — SW_DUTY8 11
VCC — 1K R59 — SW_DUTY4 10
VCC — 1K R58 — SW_DUTY2 9
VCC — 1K R56 — SW_DUTY1 8

GND

BLOCK LENGTH

SW3 ERG10412

0	0 BYTES
1	1 BYTE
2	4 BYTES
3	16 BYTES
4	64 BYTES
5	256 BYTES
6	1 KBYTE
7	2 KBYTES
8	4 KBYTES
9	8 KBYTES

VCC — 1K R61 — SW_LEN8 7
VCC — 1K R63 — SW_LEN4 6
VCC — 1K R62 — SW_LEN2 5
VCC — 1K R60 — SW_LEN1 4

GND

CLOCK FREQUENCY

SW4 ERG10412

0	66 MHZ
1	33 MHZ
2	16 MHZ
3	8 MHZ
4	4 MHZ
5	2 MHZ
6	1 MHZ
7	500 KHZ
8	250 KHZ
9	PATTERN_GEN

VCC — 1K R65 — SW_FREQ8 3
VCC — 1K R67 — SW_FREQ4 2
VCC — 1K R66 — SW_FREQ2 1
VCC — 1K R64 — SW_FREQ1 0

GND

ROT_SWITCHES<15..0>

PATTERN GENERATOR

J5 — VROUD2X10

PG0	1	2	ST3
PG1	3	4	ST4
PG2	5	6	ST5
PG3	7	8	ST6
PG4	9	10	ST7
PG5	11	12	ST8
PG6	13	14	ST9
PG7	15	16	ST10
	17	18	
	19	20	

VCC — 1K R70 — PAU — PG0
VCC — 1K R71 — PAU — PG1
VCC — 1K R72 — PAU — PG2
VCC — 1K R73 — PAU — PG3
VCC — 1K R74 — PAU — PG4
VCC — 1K R75 — PAU — PG5
VCC — 1K R76 — PAU — PG6
VCC — 1K R77 — PAU — PG7

PATT_GEN<0> 0
PATT_GEN<1> 1
PATT_GEN<2> 2
PATT_GEN<3> 3
PATT_GEN<4> 4
PATT_GEN<5> 5
PATT_GEN<6> 6
PATT_GEN<7> 7

PATT_GEN<7..0>

GND

VCC — 390 R90 — RUN_LED_BUF

START/STOP STEP

SW11 600P

VCC — 1K R92 — STEP3
VCC — 1K R91 — STEP2

GND

INJECT ERROR

SW10

VCC — 1K R88 — INJ3
VCC — 1K R89 — INJ2

GND

AN ERROR IN SW11'S SYMBOL HAS CAUSED THE LED'S ANODE TO BE CONNECTED TO RUN_LED_BUF, THE LED'S CATHODE TO BE UNCONNECTED AND THE RESISTOR TO BE CONNECTED TO VCC AND GND.

SOLVED BY INVERTING THE SIGNAL RUN_LED_BUF IN THE ALTERA AND SOLDERING R90 TO THE CATHODE OF THE LED AND GND.

DATA ERROR

SW6 SECME1K2

VCC — 1K R79 — DERR3
VCC — 1K R81 — DERR2

GND

CNTL ERROR

SW7

VCC — 1K R82 — CERR3
VCC — 1K R83 — CERR2

GND

FEMB / LDC

SW8 SECME1K2

VCC — 1K R84 — FEMB3
VCC — 1K R86 — FEMB2

GND

LDOWN

SW9 SECME1K2

VCC — 1K R85 — LDOWN3
VCC — 1K R87 — LDOWN2

GND

BLOCK / WORD ERROR DET.

SW5 SECME1K2

VCC — 1K R78 — BLOCK3
VCC — 1K R80 — BLOCK2

GND

DRAWING SLIDAS
LAST_MODIFIED=Mon Mar 10 15:05:34 1997

REF: SLIDAS.LOGIC.1.1

CERN CN/CE
DIV. ECP EDU/DQ
1211 GENEVA 23
SWITZERLAND

TITLE: S-LINK DATA SOURCE

ABBREV: SLIDAS | PAGE: 1/3

FILE: S-LINK/SLIDAS/PCB/680-1110-500/SLIDAS/LOGIC.1.1

DESSIN: PH.BRODIER-Y. | ETUDE: | DATE: