S-LINK: A Prototype of the ATLAS Read-out Link

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Abstract

The ATLAS data acquisition system needs over 1500 read-out links between the read-out drivers and the read-out buffers. As it is too early to define the physical layer of those links, the S-LINK specification has been written. It defines a media independent 32-bit synchronous FIFO-like interface for both the sender and receiver side of a link. S-LINKs can send control and data words, can detect link errors and have a self-test mode. Fibre-optic gigabit versions of S-LINK are used by various ATLAS detectors as prototype read-out link and also as trigger information distribution link.

1. INTRODUCTION

The ATLAS data acquisition system [1] (Figure 1) needs many different types of links. The links that move raw digitised data out of the detector are called front-end links. About 50 000 of those links are needed; they will have a length of about 80 m, and move the data to an area without radiation where the read-out drivers (ROD) are located.

The front-end links are not standardised: some detectors use electrical transmission with a rate of 40 Mbps while others use transmission over optical media with rates of 1 Gbps or 1.6 Gbps. The RODs, which are specific to each detector, will format the data so that all detectors send similar structured data streams to the read-out buffers (ROB) where the data will be stored until a level-2 trigger decision has been made.

For cost and support reasons it is desirable to minimise the amount of different elements in the final DAQ system. The read-out link is a logical location to go from detector specific logic to standard logic. The ATLAS Trigger-DAQ Steering Group therefore has specified [2] that a standard read-out link specification will be used. In total about 1500 of these 200 m long links are needed, while the average data rate over each link is in the order of 100 MByte/s.

Although there is a requirement for a standard read-out link specification, link technologies are changing too rapidly to specify the physical layer of the read-out links already now. On the other hand designers of the RODs and ROBs have to build systems for testbeams in order to work towards the final system. To cope with this problem the S-LINK specification [3] has been written.

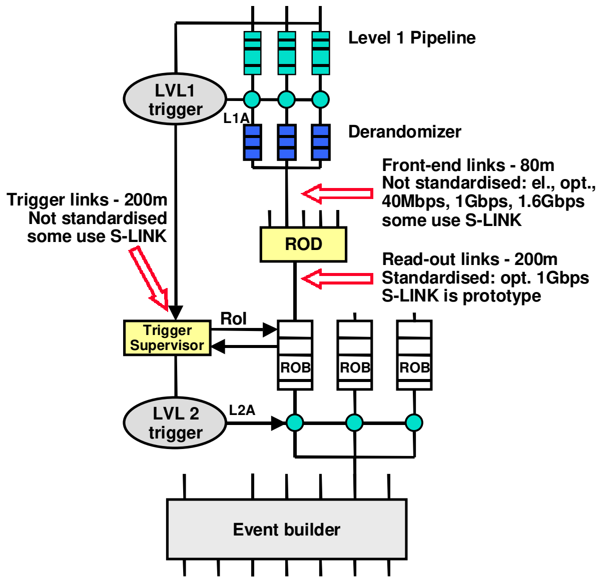

Figure 1: ATLAS DAQ

2. S-LINK OVERVIEW

The idea of S-LINK is that, unlike other standards that define the physical layer, it defines a simple FIFO-like interface (Figure 2) on which the use of the signals remains independent of the technology used to implement the physical link. The mapping of the S-LINK signals to the protocol used on the physical link is left open to the designers of the links, allowing them to map it in the most suitable way for the technology used.

To allow interchangeability of different implementations of S-LINK cards, the specification recommends the use of small daughter boards. A single, high-density, 64-pin connector connects the ROD to the Link Source Card (LSC) and the Link Destination Card (LDC) to the ROB. Both the format of the daughter board and the type of connector used correspond to the IEEE Common Mezzanine Card standard, which is the same format as used by PCI Mezzanine Cards (PMC). This daughter card implementation should be used during the prototyping phases, while for the final systems the link logic may be integrated onto the motherboards.

Both LSC and LDC are designed by one group. With this approach the link, including both link cards, can be treated as a component in the system, which offers the advantage of having well defined inputs and outputs.

This means that various implementations of S-LINK (copper, fibre optic, standard or radiation tolerant components) can be developed using new technologies, independently of the design of the RODs or the ROBs.

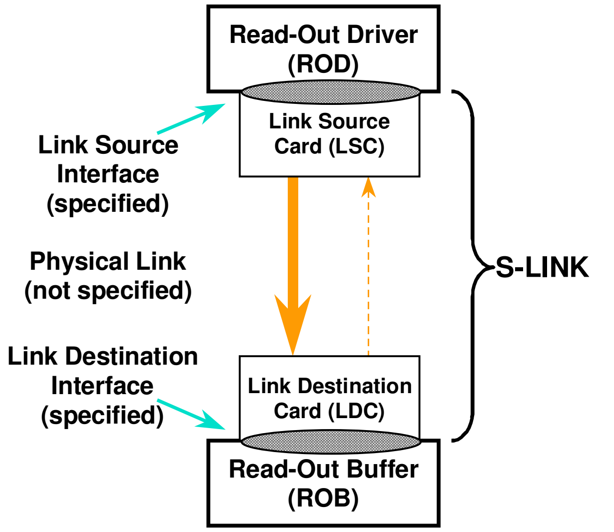

Figure 2: S-LINK concept used in read-out link

With the plug-in cards, S-LINK relieves the ROD and ROB designers from making high-speed designs having signals with frequencies of 500 MHz and more. It also means that a designer may change from one link technology to another without needing to modify the motherboards. Apart from that, the S-LINK specification adds important features to the direct use of basic link components:

- detection of bit errors
- start/end of event control words
- generation and checking of a known test pattern
- optional flow control
- controlled reset

Other links that may benefit from this standard link interface approach are the front-end links and the links used in the trigger system.

3. S-LINK DEVICES

Today two types of link cards exist: one based on Fibre Channel technology (Figure 3) [4], capable of moving data serially at 103 MByte/s over 500 m fibre-optic or 30 m electrical media and another based on parallel electrical transmission over a 10 m SCSI cable [5].

These link cards are implemented as plug-in modules. For final applications the link electronics may be integrated into the ROD and ROB designs. We are testing such an integration procedure (Fibre Channel S-LINK integrated with S-LINK to PCI) to see if there are any complications in copying the high-speed design with other CAD tools and PCB layouts.

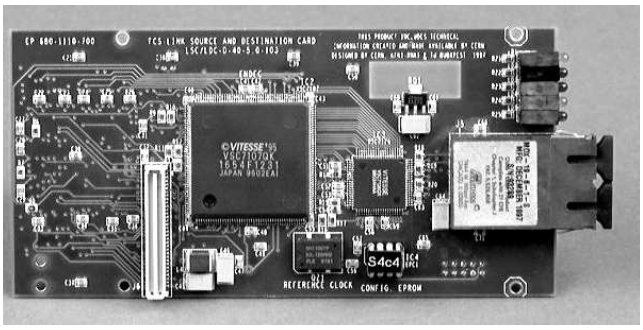

Figure 3: Fibre Channel S-LINK

S-LINK interfaces to PCI and PMC have been built to be able to read out data using standard PC's or VME boards. Those interfaces can receive data at the maximum link speed of 103 MByte/s, while with the SLIDAS data generator test tool a speed of 117 MByte/s into a PC memory has been measured. The PCI and PMC to S-LINK interfaces can transmit data at maximum 65 MByte/s.

An integral part of the S-LINK project has been the design of test tools. High speed data generators (up to 160 MByte/s), data sinks, link testers and logic state analyser setups have been made.

All S-LINK designs, including the test equipment, are available from industry. For final applications the schematic diagrams and programming files are available so that the designs may be integrated to reduce the cost and increase the reliability.

4. ATLAS APPLICATIONS

4.1 DAQ Prototype-1

The ATLAS DAQ/Event Filter Prototype -1 Project (DAQ-1) [6] is producing a prototype system representing a "full slice" of a DAQ suitable for evaluating candidate technologies and architectures for the final ATLAS DAQ system.

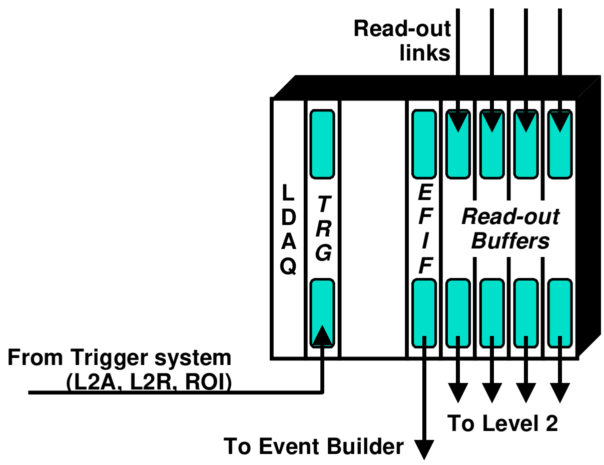

Figure 4: ATLAS Read-out Crate

In this project S-LINK is used as the prototype of the read-out link. Currently, in the Read-out Crate, a CES RIO2 with an S-LINK to PMC interface is used to emulate the ROB (Figure 4). A LynxOS library [7] has been written and performance measurements have been made [8]. For simple ROB applications implemented on a RIO2/8062, an event handling frequency between 36 KHz and 67 KHz have been measured for event sizes of 1084 and 64 bytes respectively. Maximum performance measured on this platform is 72 MByte/s for packet sizes of 8 KByte or more, with an overhead of 8µs. Those tests have been made with the SLIDAS test tool which can generate full-speed ROD-like data. Also programs that can emulate ROD data to be fed into the read-out crate have been made to test the functionality of the system without needing a real detector or ROD.

The DAQ-1 project has also defined the format of the data that is sent over the read-out link (Figure 5)[9]. For ease of implementation and cost reasons, the dataformat is designed in such a way that the ROD may be implemented easily in hardware, i.e. without the need for processors or large storage. The dataformat includes both a header and a trailer, and uses the ability of the link to transfer control words to signal the start and end of each event.

Beginning of Block control word
Start of Header Marker
Header Size
Format Version No.
Source Identifier
Level 1 ID
Bunch Crossing ID
Level 1 Trigger Type
Detector Event Type
Data or Status elements
Status or Data elements
Number of status elements
Number of data elements
Data/Status First Flag
End of Block control word

Figure 5: Draft Read-out Link data format

4.2 ROB-in

The Royal Holloway / University College of London has designed the input stage of the ROB, called the ROB-in [10]. The PCI board (Figure 6) contains an INTEL i960RP processor with a PCI interface and a 512 KByte memory which stores the event data. Data coming from S-LINK is written directly into the memory without needing any intervention of the processor. The processor is mainly used for memory management and for handling Region of Interest request messages.

Performance measurements with the SLIDAS data generator show that the input to memory can sustain a speed of 130 MByte/s. With an event size of 1 KByte, the processor can handle the event data at a rate of 75 KHz. The new version of the board will use an i960RD processor, which runs internally at 66 MHz. It is expected that this board will be able to run at the rate of 100 KHz that the final ATLAS system requires. One prototype of the ROB-in board is in use in the ATLAS DAQ/Event Filter prototype - 1 project. A PMC version of the board is being manufactured which better fits the VME environment that is used in the project.

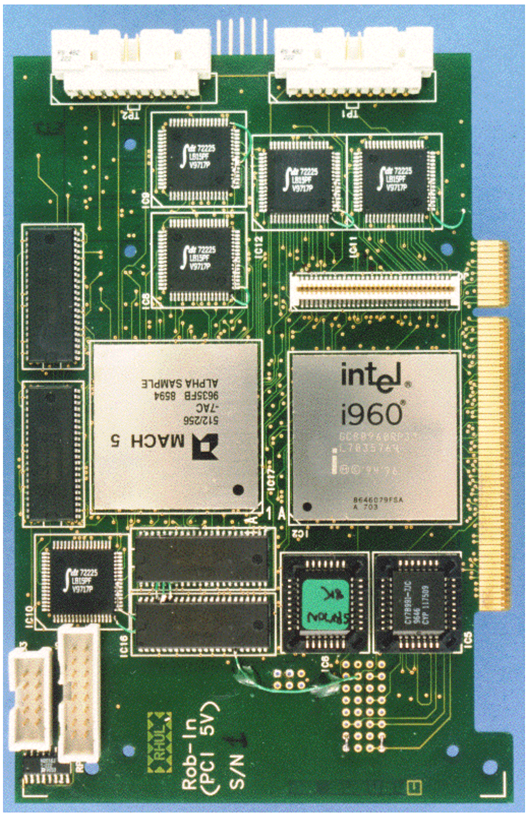

Figure 6: PCI version of ROB-in with S-LINK connector

4.3 Transition Radiation Tracker (TRT)

The block diagram of the Transition Radiation Tracker (TRT) read-out driver (Figure 7) [11] shows a typical ROD design. Links from the read-out chips running at 40 Mbps using LVDS levels are connected to the readout part (RD). The outputs from the RDs are connected to Zero suppression (ZS) circuitry and buffer.

The clock and data are received from the Trigger module through the Trigger Module Interface. The header of the event, which follows the ROD data format (Figure 5), is generated at the Header Generator part using headers from the read-out chips and data from Trigger Interface.

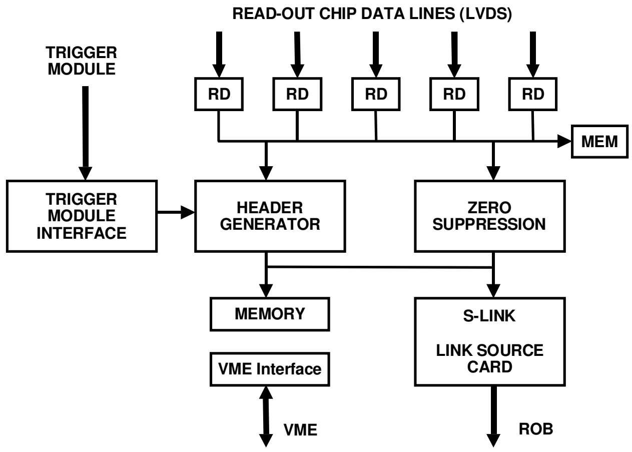

Figure 7: TRT ROD

There is another buffering after ZS to be able to verify data before and after ZS. The complete event is fed to the S-LINK LSC. To make the board and a final system easy to debug, test patterns can be injected into the RDs and into the header generator.

A prototype is now working, while a complete TRT ROD with S-LINK output is expected to be ready by the middle of 1999.

4.4 Calorimeter trigger ROD

The ROD of the Level-1 Calorimeter Trigger [12] collects data from level-1 accepted events over a pipeline bus and sends them via an S-LINK interface to a ROB. The pipeline bus was designed to match all important aspects of the S-LINK hardware: e.g. both interfaces employ a FIFO concept with a 32-bit bus and they are clocked with the same clock frequency of 33 MHz. The data is already received on the ROD in a sequential order. The ROD adds an event header and trailer to the data set and stores it in a FIFO memory until it can be transmitted with the S-LINK to the level-2 buffer. In total eight to sixteen S-LINKs will be needed.

4.5 Monitored Drift Tube (MDT)

The first detector to use S-LINK for the readout was the Monitored Drift Tube detector (MDT) [13]. In 1997 it used the test beam at H8 in which the data was read out over a fibre-optic S-LINK and an S-LINK to PMC interface plugged on a RIO2. This card in turn was read out by the RD-13 DAQ software which still is the standard software for test beams.

They could either read the outputs of the discriminators over analog links into Time to Digital Converters (TDC) in a VME crate, or they could use the TDCs which are on the chamber and read the digitised data out over S-LINK. In both the 1997 and 1998 testbeams the two systems have been used in parallel. In this application S-LINK is actually used as a front-end link.

NIKHEF designs the MDT ROD, called NIMROD (Figure 8). The NIMROD version with an S-LINK output is expected to be ready by the middle of 1999.

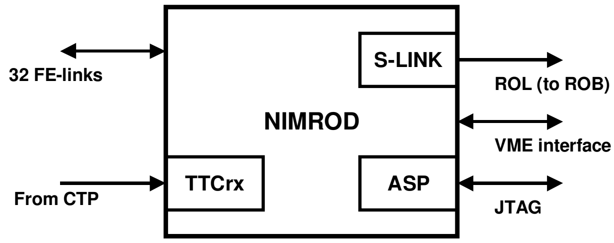

Figure 8: NIMROD connections

4.6 TileCal

In August 1998 the ATLAS TileCal became the second detector to use S-LINK as the front-end link [14]. The DAQ system looked similar to the one from the MDT. They read out both over S-LINK and with separate digitiser/ADC cards. The data from the two read-out paths matched very closely except for some gain differences between the two different digitiser cards. In total more than 100.000 events have been read out over S-LINK, which corresponds to a few GByte. The maximum rate data was taken into RIO2 was 15 KHz with 2 KByte events. This includes processing of the data in the RIO2.

4.7 Trigger supervisor

The ATLAS Trigger Supervisor [15] uses S-LINK as a trigger link. It dispatches level-1 trigger information describing the regions of interest (ROI) to the level-2 processing farm and the ROBs. Currently the way it accomplishes this is through a processor farm coupled with hardware assisted buffered I/O. On the input to the Supervisor there is an S-LINK connection from the level-1 system that provides a transmission per event with the level-1 data needed by the Supervisor. The Input S-LINK Distributor buffers and dispatches this data (which arrives at a maximum rate of 100 kHz) to one of several PMC cards attached to the Supervisor processors (one PMC per processor). The processors send requests to the ROBs via the same PMC connection. The S-LINK Distributor buffers the requests and intelligently fans the requests out to a number of S-LINK channels (one per ROB crate in the current scheme). This application also uses the ability of S-LINK to send control words.

A prototype of the Trigger Supervisor was built and has been used in several level-2 demonstrator systems. In those demonstrator systems, the level-1 input was emulated by a RIO2 with an PMC to S-LINK card. With a single processor, an event handling rate of 27 KHz has been shown. As the system is scalable, with only five processors the final ATLAS requirement of 100 KHz can readily be met.

5. APPLICATIONS OUTSIDE ATLAS

S-LINK is also used outside ATLAS. The COMPASS experiment will use 200 commercial fibre-optic S-LINKs and has built an S-LINK to PCI interface with a large buffer memory that can hold all data from one spill [16]. The COMPASS equivalent of a ROD is the CATCH-X board. It has 16 HOTLINK inputs and one S-LINK output; a prototype in VME format with four HOTLINK inputs will be ready by the end of 1998.

Applications outside HEP such as the ASDEX Upgrade fusion experiment and the MegaPrime astronomy camera have advanced plans to use S-LINK. Since 1997 the Olivetti and Oracle Research laboratories use S-LINK in combination with Linux drivers for moving video and keyboard data to and from remote terminals.

6. FUTURE

As the Muon Trigger and Tile Calorimeter are planning to use S-LINK as the front-end link, there is a requirement of making a radiation tolerant version. We will build such a version if a suitable serialiser chip is selected by the ATLAS front-end link working group. In preparation of this we are investigating radiation tolerant programmable logic chips. When this rad-tol version is available, link users may just replace the link card without modifying their own hardware as all S-LINK link cards are compatible. Another project will try out a method to have S-LINK inputs on the rear-side of VME crates, as this can solve both wiring and cooling problems that may arise in a large scale setup. Other ongoing projects aim to reduce the cost of the physical links by using components of more popular technologies like Gigabit Ethernet. Last but not least, a major part of the S-LINK project will continue to focus on supporting users by performing design reviews and loaning equipment.

7. CONCLUSIONS

The S-LINK specification describes an easy-to-use datalink which relieves read-out designers from the task of designing high frequency transmission circuits with error detection capabilities. Links, interfaces and test tools have been designed and are commercially available. S-LINK has been used already in several applications within ATLAS, other experiments and also outside high energy physics. Considerable knowledge and experience with the links, test tools and software has been built up, while also the robustness of the cards and tools has been proven. Ongoing efforts are being made to reduce the price of the links, to make a radiation tolerant version and to allow easier integration into large scale systems. Furthermore extensive support is given to projects inside and outside ATLAS that want to incorporate S-LINK (http://www.cern.ch/hsi/s-link).

8. REFERENCES

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