A Front End Digitization and Readout System for the ATLAS Level-1 Calorimeter Trigger

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Abstract: *A digitization and readout system for the ATLAS calorimeter level-1 trigger is presented. As an essential part a custom made ASIC has been built and tested which incorporates the functions of initial data processing, including transverse energy calibration and bunch crossing identification (BCID), and the fast read out of level-1 accepted event data via a sequential I/O interface. The complete system will be able to receive analog data from the detector, to deliver high speed digitized data to the level-1 trigger processor and to provide a readout of trigger data to be used at higher trigger levels or in the off-line data analysis.*

1 Introduction

The architecture of the level-1 calorimeter trigger front end depends on the choice of the calorimeter readout system. An analog pipeline readout or a FERMI system [LHCC-95-56a] with large delay for processing of level-1 trigger data require a separate digitization system for the level-1 calorimeter trigger [LHCC-94-43]. The requirements for the front end digitization system may be summarized as follows:

- Sum calorimeter signals in order to form trigger towers of 0.1×0.1 in $\eta - \phi$-space, and for the electro-magnetic/hadronic sections in longitudinal direction.
- Transmit analog signals to the trigger electronics over 80 m.
- Digitize the analog signals with 8-bit resolution[1] at 40 MHz.
- Perform pedestal subtraction and energy calibration using a lookup table (LUT).
- Carry out Bunch Crossing Identification (BCID).
- Transfer the trigger data to calorimeter algorithm modules by means of high speed digital links.
- Provide an internal data source for testing the trigger.
- Read out the raw digitized trigger data.

The digitized calorimeter trigger data are only visible to the trigger system. It is therefore mandatory to look upon the calorimeter level-1 trigger as an independent detector component which has to be read out. The raw data are necessary for trigger calibration and monitoring. These data are also accessible from the level-2 trigger.

The following chapter gives a general overview of the digitization and readout system for ATLAS level-1 calorimeter trigger. A first mapping of trigger channels to trigger front end modules is proposed while a detailed segmentation scheme depends on the result of a demonstrator project. For the demonstrator we implement the full functionality of the system for a reduced number of channels per design component. Chapter 3 gives a detailed description on Front End ASIC for the demonstrator project, which has been already designed and successfully tested. The next step in the demonstrator program will be the design of the readout merger ASIC, which is described in chapter 4. We will report on the design of a first multi chip module in a forthcoming publication.

2 Architecture Overview

Our design approach concentrates on the processing and readout functions of the trigger digitization

[1] A digitization system with 10-bit resolution is also taken into consideration

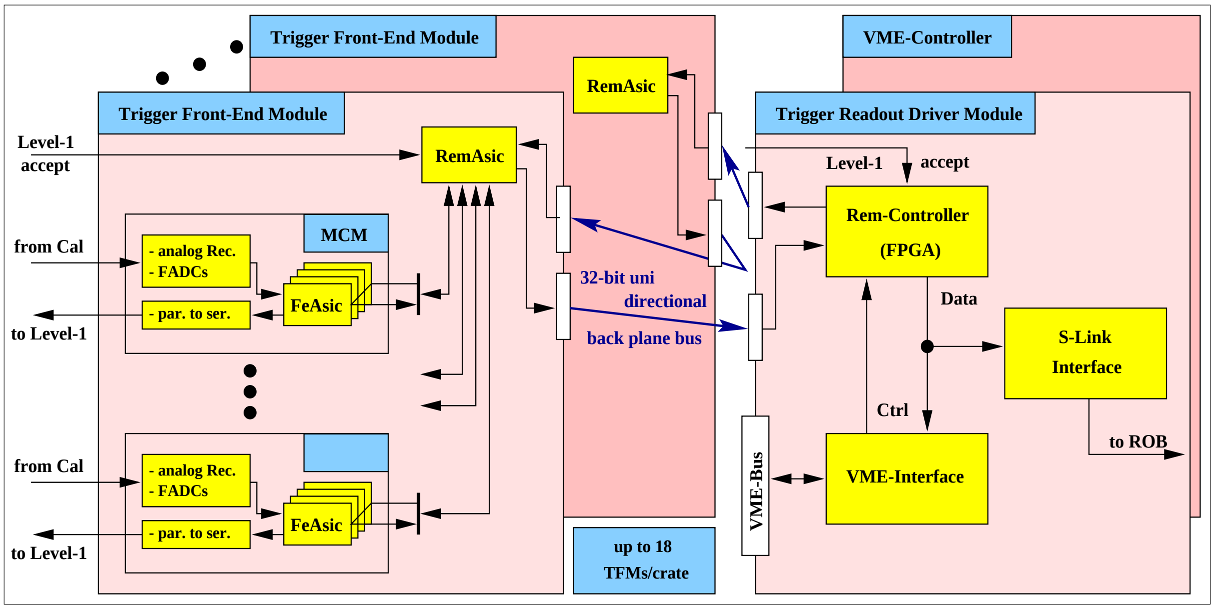

Figure 1: Block diagrams of modules for the level-1 calorimeter digitization and readout system

system. Details on the analog trigger tower summation are under investigation in the LAr working group. Studies on the analog signal transmission system are published in [HD-IHEP-96-16, LHCC-95-56c].

We have learned from the development of a trigger FADC in the RD27 collaboration [LHCC-96-4] that a discrete design approach would cause an unacceptable size of the digitization system. With the development of the BCID-ASIC [LHCC-95-56b, LHCC-95-56c] we gained confidence, that dedicated ASICs for trigger data processing and readout can be designed on a short time scale leading to a flexible and affordable system. We also plan to use the Multi Chip Module (MCM) technique to improve the scale of integration further.

Figure 1 shows the proposed digitization system based on VME-boards called Trigger Front End Modules (TFM). The TFM boards are equipped with analog receivers for 96 of the (2×4096) trigger tower channels from the electro-magnetic and hadronic calorimeter. An 8-bit FADC digitizes the calorimeter pulses with an LSB equivalent of 1 GeV at 40 MHz. The energy data are calibrated and the bunch crossing of the calorimeter signal determined. This initial data processing is implemented as a pipelined circuit. Data of two trigger towers are then converted to a serial format and sent to the calorimeter trigger algorithm modules. A digital pipeline stores data for the readout during the level-1 trigger latency. On a level-1 accept the data are copied to a derandomizer buffer. This derandomizer buffer stores the data during the readout process which lasts in the order of a few μsec per event.

The digital processing and readout components will be integrated on an ASIC, the so called Front End ASIC (FeAsic). In the final design each FeAsic will receive data from 4 trigger towers. The FeAsics could be integrated together with analog receivers, FADCs and the parallel to serial converter on MCMs. The FeAsic has a sequential I/O interface. The I/O interfaces of the FeAsics on a MCM can be coupled to operate in daisy chain configuration.

The FeAsics of all MCMs on one TFM are connected to a second ASIC, the Readout Merger ASIC (RemAsic). The FeAsic data format will include run time information, like pipeline addresses, to allow a check on the synchronous running condition of the TFMs. The merged data are compressed to reduce the otherwise necessary bandwidth for the whole system of 6.4 GBit/sec. The data of all TFMs are read out over a 32 bit uni-directional back plane bus.

The bus design is based on a token ring concept with the RemAsics acting as nodes in the ring. A

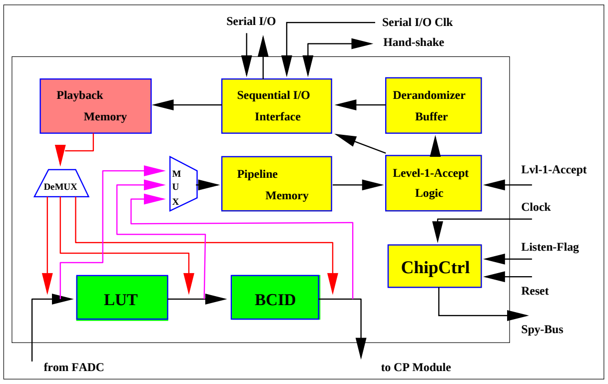

Figure 2: Block diagram of the Front End Asic (FeAsic)

bus interface (configured in a FPGA) on the Trigger Readout Driver Module (TROD) submits tokens to initiate readout or control operations. The bandwidth of the 32 bit bus is of the order of 1 GBit/sec at 33 MHz clock frequency. The bandwidth can be increased by operating several token rings in one crate. The performance of the back plane is tuned to the S-Link hardware which is foreseen to be the transfer link between the TROD and level-2 readout buffer (ROB) in ATLAS. The token ring bus as well as the S-Link act as FIFOs, hence the amount of memory and memory management required on the TROD can be kept to the minimum.

For a demonstrator project we have designed a FeAsic prototype for processing and readout of one trigger tower. A VME module is currently under construction incorporating 4 FeAsic prototype chips, which receive digitized data from a RD27 FADC and transmit the level-1 trigger data via a high speed digital interface (G-Link) to the Cluster Processing Modules [LHCC-95-56d]. It will be used to gather experience with the readout of events at 100 kHz level-1 trigger rate. In the second stage we will design the RemAsic for reading 16 FeAsics prototype chips. In parallel we want to investigate the MCM technology. A MCM prototype is planned for 4 trigger towers until the end of 1997.

3 Front End ASIC (FeAsic)

Figure 2 shows the block diagram of the FeAsic. The bottom blocks in dark grey indicate the initial level-1 trigger processing components, which consists of the calibration LUT and the bunch crossing identification (BCID) circuit. The data to be read out can be picked up from three different locations in the processing pipeline. The components of the readout system are shown in the light grey blocks. Readout and control operations on the FeAsic are done through the sequential I/O interface. A playback memory (256×10) bit can be used as internal data source for testing the FeAsic itself and/or the subsequent trigger logic. The internal data source can be coupled at three positions into the processing pipeline.

The FeAsic design was described in the VERILOG Hardware Description Language and realized in the ES2 0.7 μm CMOS process. The design required static RAMs and dual ported RAMs, which were created using a macro cell generator that is part of the ES2-library. The design consists of about 3000 standard cells as well as 1.2 kByte of memory. Its implementation required 80000 transistors on a 16.4 mm^2 silicon die (Fig. 3). We conclude from the compact design for one trigger channel that with the current technology at least 4 trigger tower channels can be integrated onto a final FeAsic.

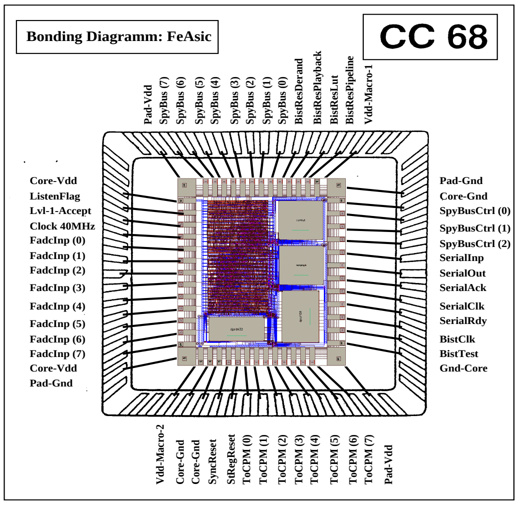

Figure 3: Bonding diagram of the FeAsic

3.1 Initial Level-1 Trigger Data Processing

The first step of the data processing are a precise weighting in transverse energy (E_t) and pedestal subtraction, which are performed by using a LUT. The signals produced by the calorimeter span several bunch crossings. The role of the BCID filter is to identify the sample containing the peak of the calorimeter pulse, and to pass on data for this sample only. The analog shaping of the signals guarantees a fixed time correlation between this peak sample and the bunch crossing, which produced the event. All other samples of the signal are suppressed to zero.

We used a RAM with 8 bit address and 10 bit data word as LUT. The current trigger design assumes a linear analog transmission scheme between the detector and the trigger electronics. This limits the energy range in the trigger to 256 GeV due to the 8 bit FADC and a LSB equivalent of 1 GeV. Signals above this range saturate in the trigger. As a consequence the BCID-filter becomes less efficient if more than one bin of a digitized pulse saturates. In a second scenario the analog signals can be compressed for instance using a logarithmic transfer function. The nonlinear transfer characteristic has to be linearized for the trigger electronics. In the present approach the FeAsic works internally with a 10 bit data bus. Keeping an LSB of 1 GeV it seem natural to compress the calorimeter signal for a dynamic range of 1 TeV, which can be digitized by an 8 Bit FADC. The linearization of these signals takes place in the LUT. This would allow to operate the BCID filter properly up to energies of more than 1 TeV.

The bunch crossing identification algorithm, that has been implemented, consists of a FIR-filter followed by a peak finder. The calorimeter pulse is stored in a shift register until the the decision of the peak finder. The FIR-filter is implemented with the fixed coefficients (-1, 0, 4, 0, -1) and works as peak enhancer. In the final system we plan to replace the fixed coefficient multipliers by barrel shifters in order to respond flexibly to the different pulse shapes coming from different ATLAS calorimeters. The use of integer multipliers is possible, but would need a large die surface and is hence expensive. The peak finder compares the current with the preceding and succeeding FIR-filtered data sample. Four different peak finders are implemented and can be selected ($<>, <\geq, \leq>, \leq\geq$). In the current level-1 trigger design the input to the trigger algorithm modules has a dynamic range of 8 bits. If values of the internal 10 bit bus exceed this range, they are clipped to the 8 bit maximum.

The level-1 trigger data processing are implemented as a pipelined circuit. A level-1 trigger data sample propagates in 9 clock cycles through this pipeline before it is sent to the algorithm modules. The 9 cycles are mapped onto the initial trigger data processing pipeline as follows: One clock cycle for the LUT; five data samples have to be stored in the shift register as input to the FIR-filter; another two clock cycles are necessary to store the FIR-filtered data for the peak finder. The processing pipeline terminates with an output latch to allow a clock synchronized data output for the subsequent circuit.

3.2 Digital Pipeline and Readout Interface

The Readout part of the FeAsic consists of a digital pipeline memory, a derandomizer buffer and a sequential I/O interface. Two different readout modes have been implemented. In the "stop mode" the level-1 accept signal freezes the pipeline memory and the data of successive pipeline cells can be copied to the sequential I/O interface, see Fig. 2. In the "fast readout mode" one or several consecutive data samples can be copied on a level-1 accept into the derandomizer buffer. Between the storage of 1, 4 or 8 data samples can be chosen. If more than 1 data sample is stored, checks of BCID operation and of phase relation between the FADC clock and the maximum of the analog signal are possible.

The pipeline memory is a dual ported RAM with 7 bit address and 10 bit data bus. It is used as a scrolling memory with a write and a read port. The write and a read addresses are running in parallel (synchronous FIFO). The difference between the address counters is programmable and determines the latency of the pipeline.

The derandomizer is foreseen to compensate statistical fluctuations of the level-1 accept signal. This buffer is necessary since the readout time per event is of the order of a few μsec. In order to control the dead time, the level-1 trigger generates only 16 level-1 accepts in 16 μsec. That means, the storage depth of the derandomizer buffer should be at least 16 events to ensure that no additional dead time is produced by the readout system. The derandomizer buffer of the FeAsic has 32 data slots, to allow storage of several events if more than 1 data word per event is to be read out. The derandomizer buffer is realized as asynchronous FIFO using a dual ported RAM. Each data slot is 23 bits long. It stores the 10 bit calorimeter energy data word; the 7 bit read address pointer from the pipeline memory as run time information; a 2 bit counter for monitoring derandomizer overflows and 2 bits to identify the readout mode.

The FeAsic is connected to a readout and control unit the RemAsic via the sequential I/O interface. The backbone of this interface is a 23 bit register with internal parallel read and write access. The latches can be concatenated to a shift register for the I/O operation. A separate input and output channel allows daisy chaining several I/O interface. A separate shift register clock determines the speed of the sequential I/O operation. The interface is operated by a hand shake protocol. The readout of 4 daisy chained prototype FeAsics requires 2.3 μsec with a 40 MHz shift register clock. This increases to 5.1 μsec per event in the final configuration with 4 daisy chained FeAsics where each FeAsic reads out 4 trigger towers.

3.3 Test Results

The chip was extensively tested using a HP 82000 chip tester. The sequential readout and programming interface works. The separate clock of the sequential I/O interface allows proper operation up to 140 MHz. At maximum speed the readout of a single FeAsic completes after 250 nsec. The internal data source was used to successfully test the LUT and BCID operation. The whole chip works properly at a system clock frequency of 40 MHz. The maximum applicable system clock frequency is above 80 MHz.

4 Readout Merger ASIC (RemAsic)

The RemAsic acts as interface between the FeAsics and the custom back plane bus. Figure 4 shows the block diagram of the design. The RemAsic has several sequential I/O ports. Each port will be connected to a set of FeAsics with their sequential I/O interfaces coupled in a daisy chain. The data from the FeAsics include the pipeline address as run time information. A cross check between these addresses proves that the readout system is running synchronous. The data are copied to a buffer before the data volume is reduced in a compression unit. These data are stored until a readout request from the bus interface is received. The bus interface serves also as receiver of control tokens for the RemAsic and the connected FeAsics.

The following example discusses typical data rates in a RemAsic and a trigger Readout crate. Assuming a digitization system with 96 trigger towers per TFM. The data volume from the FeAsics amounts including the headers to 800 bit per event if one data sample is read out. That means event buffering is no problem on the RemAsic. Buffer space can be implemented for the storage of more than 20 events. Assuming further that each crate contains 18 TFMs, the raw data volume adds up to 14.4 kBit per event and crate. At a level-1 trigger rate of 100 kHz a digitization system would have to transfer a raw data volume of 1.44 GBit/sec per crate. This example shows, that data compression is necessary and that a powerful custom bus is required with a transmission bandwidth of about 500 MBit/sec.

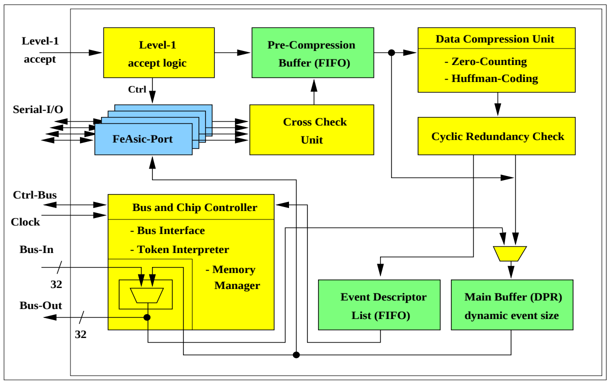

Figure 4: Block diagram of the Readout Merger Asic (RemAsic)

The data compression happens in two steps. First, the compression unit inspects how many consecutive trigger towers show a "0" GeV response in the readout. Their energy values are replaced by a Zero-token followed by the number of cells without energy. Second, all binary energy values and the Zero-token combined with the number of zero energy towers are converted to Huffman codes. A Huffman coded data concept requires an error detection mechanism, because data transmission errors would not only result in the corruption of single codes but would effect the whole data set. The cyclic redundancy check sum algorithm allows the detection of errors in data sets, while the additional overhead of check data are kept to a minimum.

The TFMs are connected to the TROD via a custom back plane bus. The bus concept is tuned to the data transfer technology between the TROD and the level-2 buffer (ROB). Therefore we plan to use a S-Link driver with a clock frequency of 33 MHz. The S-Link behaves like a FIFO for 32 bit data words. A 32 bit uni-directional bus with a token protocol could be seen as the extension of the S-Link concept to the readout bus. The readout of an event would look in such a system as follows: On a level-1 accept the bus controller on the TROD submits an event readout token to the custom bus. The token is latched in a shift register and interpreted by the RemAsic on the first TFM. On the next clock cycles the data token is sent to the next TFM and the RemAsic appends its the event data. The following TFM boards interpret the token; they shift token plus the already created event data set to the subsequent board and append their own part of the event data set. The completed data set is received at the TROD and sent preceded by an event header to the S-Link driver. The theoretical bandwidth of this custom bus and the S-Link driver is of the order of 1 GBit/sec.

5 Summary

We have developed a comprehensive design for the front end of the ATLAS level-1 calorimeter trigger system.

Digitization in a commercial FADC and Bunch Crossing Identification in a custom made ASIC are already demonstrated to work within required specification. An additional and crucial aspect - the readout of raw data on the complete separate trigger data path - has been incorporated. Such a readout is mandatory for calibration of the energy scale as seen in the subsequent trigger logic. It also serves as an important monitoring tool for the adjustment of trigger thresholds to varying beam and background conditions in the LHC storage ring.

The design was driven by the need of high integration level in order to keep hardware within manageable and affordable size limits. It also applies a data reduction concept in such a way that the ATLAS data acquisition system can be interfaced to handle the data flow from the level-1 trigger system.

Acknowledgement

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